

Appl. No.: 09/492,787
Docket No.: 0879-0250P
Reply to Office Action of November 7, 2003

REMARKS

Claims 1-8 are pending in this application. Claims 1 and 6 are independent claims. By this amendment, claims 1 and 6 are amended and new claims 7 and 8 are added. Reconsideration in view of the above amendments and following remarks is respectfully solicited.

The Claims Define Patentable Subject Matter

The Office Action rejects: (1) claims 1, 3 and 5 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,130,420 to Tanaka et al. (hereafter Tanaka); (2) claims 2 and 4 under 35 U.S.C. §103(a) as being unpatentable over Tanaka; and (3) claim 6 under 35 U.S.C. §103(a) as being unpatentable U.S. Patent No. 5,206,730 to Sakai (hereafter Sakai).

These rejections are respectfully traversed.

The Claims Fail to be Anticipated By Tanaka

Applicant respectfully submits that Tanaka fails to teach or suggest each and every feature as set forth in the claimed invention.

In the present invention as set forth in claim 1, an image processing unit includes a frequency dividing device that divides a frequency of a drive clock. An A/D converting device converts an image signal outputted from an imaging device according to a drive clock into a digital image data. A signal processing part captures the digital image data outputted from the A/D converting device in synchronization with a frequency-divided clock outputted from the frequency dividing device and processes the digital image data.

The image data is thinned out upon the input of the data into the signal processing part.

For example, in the present invention the A/D converting device converts the analog imaging signal read from the imaging device into digital data synchronous with the drive clock for the imaging device and inputs the frequency-divided clock into the signal processing part when the digital data is inputted to the signal processing part. The data inputted to the signal processing part is thinned in accordance with a frequency-dividing rate since the image data is inputted to the signal processing part in synchronization with the frequency-divided clock. Thus, the pixels of the image data obtained from a single plate CCD can be thinned out without changing the arrangement of the pixels to enable a reduction of a memory capacity and reduce the consumption of electricity.

The Office Action alleges that Tanaka discloses that "the signal processor 104 captures images in synchronization with the frequency divided clock since the pixels are continually read to the signal processor (104) based on the output of the timing generator (20)." (see Office Action, page 2, paragraph 3). Applicant respectfully disagrees with the Examiner's assertions.

In contrast with the present invention, Tanaka fails to teach or suggest a relationship between the frequency of the drive clock for CCD 10 and the frequency of the timing signal.

For example, Fig. 1 of Tanaka merely teaches a frequency such as V pulse and H pulse being transmitted to the CCD 10. In Tanaka, the frequency of the reference pulse is divided by a factor of m ($1/m$, where m is a natural number). However, Tanaka fails to teach

any features of the frequency of the timing signal that is being transmitted into the A/D converter 103 and/or the camera signal processing circuit 104.

Even if one was to assume that the timing generator 21 of Tanaka outputs a timing signal to the A/D converter 103 and the camera signal processing circuit 104, Tanaka is still conceivably limited to the teaching that the frequency of the timing signal transmitted to both the A/D converter 103 and the cameral signal processing circuit 104 is divided by a factor of m , when the frequency of the drive pulse for the CCD 10 is divided by a factor of m . In other words, it seems that Tanaka's frequency of the drive pulse for the CCD 10 is also applied to the A/D converter 103 and the cameral signal processing circuit 104.

In contrast with Tanaka, in the present invention the frequency-divided clock is used to determine the timing for inputting the digital data into the signal processing part, although the A/D converter converts the analog imaging signal into a digital signal in synchronization with the drive clock for the imaging device. (see applicant's Fig. 1). In the present invention, since the signal processing part captures the digital image data in accordance with the divided clock, the image data is thinned to reduce the image data upon input of the digital image into the signal processing part. Such a feature of the reduction of the image data fails to be taught or suggested by Tanaka.

According to MPEP §2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. Of California*, 814

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F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ...claims." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913 (Fed. Cir. 1989). The elements must be arranged as required by the claims, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Applicant respectfully submits that the Office Action has failed to establish the required *prima facie* case of anticipation because the cited reference, Tanaka, fails to teach or suggest each and every feature as set forth in the claimed invention.

Applicant respectfully submits that independent claims 1 is allowable over Tanaka for at least the reasons noted above.

As for each of the dependent claims not particularly discussed above, these claims are also allowable for at least the reasons set forth above regarding their corresponding independent claims, and/or for the further features claimed therein.

Accordingly, withdrawal of the rejection of claims 1, 3 and 5 under 35 U.S.C. §102(e) is respectfully solicited.

The Claims Fail to be Obvious

Applicant respectfully submits that not only does Tanaka fails to teach or suggest each and every feature as set forth in the claimed invention, but Tanaka also fails to make the claimed invention obvious. Applicant respectfully submits that but for applicant's own disclosure of the specific features involved, the applied reference, Tanaka, would not have instructed one versed in the art on how to go about selectively reworking and modifying such

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a device to yield applicant's claimed invention. Accordingly, applicant submits that the Examiner's rejection is predicated upon impermissible hindsight, and not upon a suggestion from Tanaka that would have been derivable by one versed in the art from the reference itself.

In addition, applicant respectfully submits that Sakai fails to teach or suggest each and every feature of the claimed invention and/or make the invention obvious.

To establish a *prima facie* case of Obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 706.02(j).

The office Action alleges that Sakai discloses the claimed invention as set forth in claim 6. Applicant respectfully disagrees with this allegation.

Claim 6 recites, *inter alia*, an image processing unit including an imaging device and a timing generating device that generates a drive clock for driving the imaging device. A frequency dividing device divides a frequency of the drive clock.

An A/D converting device converts an image signal outputted from the imaging device according to the drive clock into a digital image data. A selection device selectively inputs one of the drive clock and a frequency-divided clock outputted from the frequency dividing device to a signal processing part. The signal processing part captures the digital image data outputted from said A/D converting device in synchronization with the one of said drive clock and said frequency-divided clock outputted from said frequency dividing device, and processes the digital image data. A display displays an image according to an image data outputted from the signal processing part. A recording device records the image data outputted from the signal processing part to which the digital image data is inputted in synchronization with said drive clock. The image data is thinned out upon the input of the data into the signal processing part.

In contrast with claim 6, Figs. 1 and 2 of Sakai merely shows a configuration wherein the clock frequency sent from SSG 1, which is a clock generator, is divided by frequency dividers 8 and 15, and then transmitted to the digital processing circuit 5. However, Sakai fails to teach or suggest pixels of the image data being thinned in accordance with the divided clock. Rather, Sakai merely teaches a digital still video camera wherein the frequency of the clock for signal processing is changed in accordance with a switch operating between the one shot photographing mode and the serial shot photographing mode, so as to reduce power consumption.

Applicant respectfully submits that not only does the Sakai fail to teach or suggest each and every feature as set forth in the claimed invention, but that one of ordinary skill in the art would

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not have been motivated to modify the teachings of Sakai to arrive at the claimed invention because there is no teaching or suggestion in any of the references regarding how or why one would modify such a system to arrive at the claimed invention.

Applicant respectfully submits that independent claim 6 is allowable over Sakai for at least the reasons noted above.

Accordingly, withdrawal of the rejection of claim 6 under 35 U.S.C. §103(a) is respectfully requested.

New Claims

As for new claims 7 and 8, Tanaka and Sakai also fail to teach or suggest each and every feature as set forth in these claims. For example, Tanaka fails to teach or suggest the reduction of the image data in a horizontal direction in accordance with an H pulse. In other words, neither Tanaka nor Sakai teaches the reduction of the image data in a horizontal direction.

Conclusion

In view of the foregoing, Applicant respectfully submits that the application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Carolyn T. Baumgardner (Reg. No. 41,345) at (703) 205-8000 to schedule a Personal Interview.

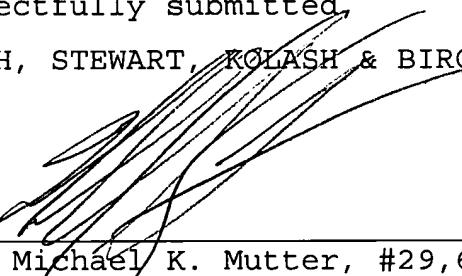
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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment from or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17; particularly, the extension of time fees.

Respectfully submitted,

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